

OTANPS SYNAPSE LINEAR RELATION MULTIPLIER CIRCUIT

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ABSTRACT

In this paper, a four quadrant VLSI analog multiplier will be proposed, in order to be used in the implementation of the neurons and synapses modules of the artificial neural networks. The main characteristics of this multiplier are the small silicon area and the low power consumption and the high value of the weight input voltage.

Keywords: analog multipliers, analog signal processing, neural networks, neurons, synapses, CMOS VLSI implementation

INTRODUCTION

Neural networks are particularly attractive for VLSI implementation as each parallel element (neuron or synapse) is relatively simple, allowing the complete integration of large networks on a single chip. Moreover, as noted by several authors, Neural Networks are most efficiently implemented by asynchronous analog circuits because they are generally faster and require less hardware (lower transistor count) than digital VLSI implementations (Mead, 1989; Mead & Ismail, 1989; Vittoz, 1994).

Hollis and Paulos (1990) present recursive Neural Networks VLSI implementations with resistive interconnections that use MOSFET analog multipliers to construct weighted sums. The network have been fabricated and successfully tested, and it is based on the Hopfield network (Hopfield & Tank, 1985). But it doesn't have the learning process.

Kub *et al.* (1990) described in their paper an analog VLSI approach for implementing an analog vector-matrix multiplier, which is completely compatible with standard VLSI technology. The feasibility for using capacitive storage for analog multiplier weight values was demonstrated. MOSFET triode multiplier circuits were described for performing analog multiplication with the analog weight values dynamically stored at the gates of MOSFET transistors. The limitation of the MOSFET triode multiplier approach is the requirement for low-input-impedance summing amplifiers.

In Saxen and Clark (1994), a four quadrant CMOS analog multiplier is presented. The multiplier uses the square-law characteristics of an MOS transistor in saturation. The active area is 10670 μm^2 . Both inputs can be varied between -0.8V and 0.8V. The problem of this multiplier is the high silicon area.

Lee *et al.* (1995) presented a four quadrant CMOS analogue multiplier based on a transconductance and a circuitry to cancel some none idealities. This multiplier has large dynamic input range, good linearity and can provide either a differential output current or voltage. These properties make the multiplier very suitable for use in the implementation of artificial neural networks. However, the complexity of the circuits and the use of many transistors and the use of the triode region not on the saturation region of the transistor is a real problem.

In Han and Sinencio (1998), a tutorial of more than 70 CMOS transconductance multipliers is presented, but these circuits are suitable for signal processing such as filter, mixers, and modulators in a communication system and some of them for neural networks.

Valle *et al.* (1996) proposed a non-linear multiplier to implement an artificial neural networks. It has an exponential relation between the output current and the weight input voltage and a small linear range relation between the output current and the other input voltage.

In order to improve the learning of the neural networks, Chiblè (1997) modified the multiplier proposed in Valle *et al.* (1996). A quadratic relation instead of an exponential relation between the output current and the weight input voltage was proposed. The multiplier proposed has been used to design an analog CMOS self-learning multilayer perceptron chip, which has been fabricated and successfully tested. The evaluation of the multiplier and their none idealities and none linearities on the behavior of the back propagation analog hardware implementation and their effect on the learning of neural networks are discussed and presented in details in Bo *et al.* (1997).

In order to achieve or to be near the ideal case, in which the neural networks can learn and work better, Chiblè (2000) modified the multiplier proposed in Chiblè (1997). A linear relation instead of a quadratic relation between the output current and the weight input voltage ($[0:5]V$) was proposed.

By reducing the supply voltage from 5V to 3.3V, and also by using the circuit as a Transconductance, Chiblè (2004) improved the multiplier proposed in Chiblè (2000). The circuit has been fabricated and successfully tested.

In Kapanoglu and Yildirim (2004), a low power-four quadrant CMOS analog multiplier for artificial neural networks is presented. The power consumption is $133\mu w$, and the power supply is 5V and the linear dynamic range of inputs is $\pm IV$.

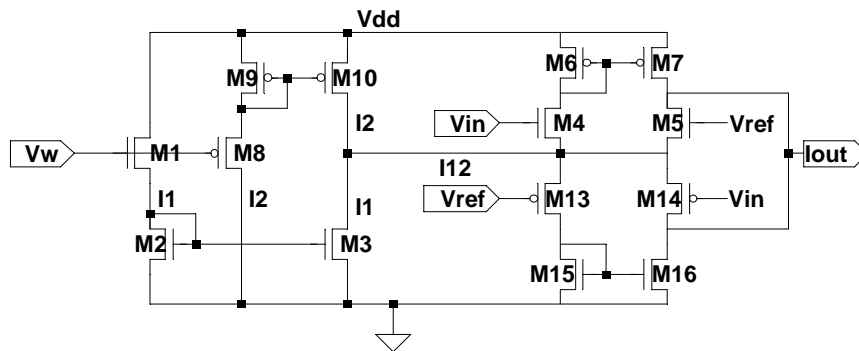
In Zhangcai *et al.* (2006), a wide dynamic range four quadrant CMOS analog multiplier using active feedback is presented with $\pm 1.8V$ input dynamic range and $\pm 2.5V$ supply voltage. It includes 20 transistors and 6 resistors and two amplifiers. It is not suitable for artificial neural network implementation.

Chiblè and Ghandour (2007) improved the multiplier proposed by Chiblè (2004) in a way to use only the same type of transistors N-type or P-type. In this case, no need to take into account the effect of electron mobility between P-channel and N-channel and also in this case the layout design time is less.

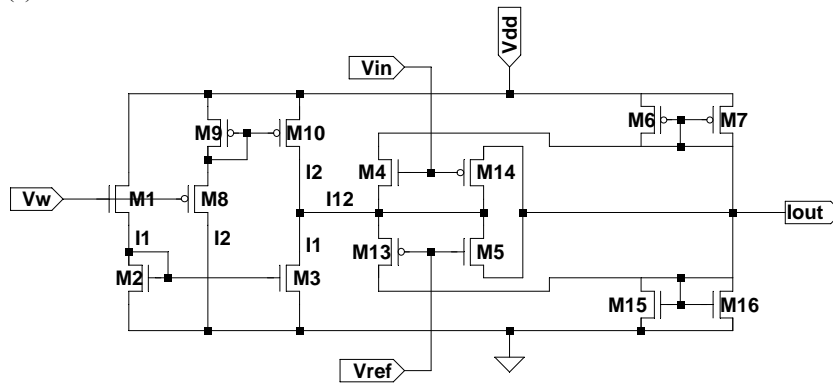
In this paper, a new version of the multiplier is proposed, in order to simplify the layout and to reduce the silicon area and power consumption. It is based on the multiplier proposed in Chiblè (2004), but the currents I_1 and I_2 can be connected together in a shortcut as it will be explained in this paper. The multiplier also can be divided into two parts: one part of the circuit can be embedded inside the synapse, and the second part can be embedded inside the neuron. This will save the area by reducing four transistors for each analog multiplier and consequently four transistors for each synapse in the neural networks. This paper includes the following sections: the OTANPS proposed multiplier circuit, the simulation results, the synapse & neuron implementation, and finally the conclusion.

THE OTANPS PROPOSED MULTIPLIER CIRCUIT

The OTANPS proposed multiplier circuit is shown in Figure 1(a). It is based on the multiplier presented in (Chiblè, 2004), which is based on OTAN “Operational Transconductance Amplifier ‘OTA’ with N-channel differential transistors” and on OTAP “Operational Transconductance Amplifier with P-channel differential transistors”. For simplifying, the circuit in Chiblè (2004) is called OTANP (OTAN & OTAP).



(a)



(b)

Figure 1. (a) OTANPS multiplier circuit; (b) OTANPS in a new form.

Circuit description

The proposed multiplier circuit is called OTANPS, because it is based on OTANP with shortcut between I₁ and I₂.

The main difference between this multiplier and the one described in (Chiblè (2004) is the direct connection or the shortcut of I₁ and I₂.

Why I₁ and I₂ are connected together? Because one of the two currents I₁ and I₂ will exist at a time: I₁ will go only to OTAN and I₂ will go only to OTAP.

The multiplier can be divided into two parts:
 The first part of the circuit can be embedded inside the synapse and it contains the following transistors (M1, M2, M3, M4, M5, M8, M9, M10, M13, and M14);

The second part can be embedded inside the neuron and it contains the following transistors (M6, M7, M15, and M16).

The advantage is to save the area by reducing four transistors for each analog multiplier and consequently four transistors for each synapse in the neural networks and globally it will save four transistors multiplied by the number of synapses.

The disadvantage is the presence of the effect of the electrons mobility due to the use of OTAN and OTAP. This effect can be vanished (other multiplier version) by using two OTAN and two N-channel transistors M11 and M12 connected to M10, as it is explained in details in Chiblè and Ghandour (2007).

To simplify the layout design and the division of the circuit in synapse and neuron modules, Figure 1(a) can be viewed in a new form as in Figure 1(b), which will be explained in next section.

Circuit equation

If M1 and M2 work in strong inversion and in saturation region, then the current I₁ is given by:

$$I_1 = \frac{\beta_n}{2n} \times (V_w - nV_{TH2} - V_{TH1})^2 \dots\dots\dots(1)$$

The derivation of this equation is explained in details in (Chiblè, 2000), where n is the slope factor usually smaller than 2 which tends to 1 for very large values of the gate voltage (Vittoz, 1994), V_{TH1} and V_{TH2} are the gate threshold voltage of M1 and M2, β_n is given by: $\frac{1}{\sqrt{\beta_n}} = \frac{1}{\sqrt{\beta_1}} + n \frac{1}{\sqrt{\beta_2}}$, β₁ and β₂ are respectively the transfer parameter of transistors M1, M2. The transfer parameter of any transistor equal to (μ*C_{ox}*W/L); μ is the carrier mobility, C_{ox} is the gate oxide capacitor per unit area, W/L is the channel width-to-length ratio. The same method can be used to calculate the current I₂ that passes in M8 and M9. It is given by:

$$I_2 = \frac{\beta_p}{2n} \times (V_w - n^2V_{dd} + nV_{TH9} + V_{TH8})^2 \dots\dots\dots(2)$$

V_{TH8} and V_{TH9} are the gate threshold voltage of M8 and M9, β_p is given by:
 $\frac{1}{\sqrt{\beta_p}} = \left(\frac{1}{\sqrt{\beta_8}} + n \frac{1}{\sqrt{\beta_9}} \right)$, β_8 and β_9 are respectively the transfer parameter of transistors M8, M9.

The currents I_{12} in function with V_w is given by:

$$I_{12} = \begin{cases} I_1 & \xrightarrow{\text{if}} (V_{TH1} + nV_{TH2}) < V_w < V_{dd} \\ -I_2 & \xrightarrow{\text{if}} 0 < V_w < (n^2V_{dd} - nV_{TH9} - V_{TH8}) \end{cases}$$

By designing well the transistors' dimensions, the following two approximations can be taken:

$$V_{ref} \approx nV_{TH2} + V_{TH1} \approx n^2V_{dd} - nV_{TH9} - V_{TH8} \quad \& \quad \beta_x \approx \frac{\beta_n}{2n} \approx \frac{\beta_p}{2n}$$

By substituting I_1 and I_2 in the above equation, then I_{12} becomes:

$$I_{12} = \begin{cases} \beta_x \times (V_w - V_{ref})^2 & \xrightarrow{\text{if}} V_{ref} < V_w < V_{dd} \\ -\beta_x \times (V_w - V_{ref})^2 & \xrightarrow{\text{if}} 0 < V_w < V_{ref} \end{cases} \dots\dots\dots(3)$$

The output current I_{out} is given by:

$$I_{out} = \begin{cases} I_{out-n} & \xrightarrow{\text{If}} V_{ref} < V_w < V_{dd} \\ I_{out-p} & \xrightarrow{\text{If}} 0 < V_w < V_{ref} \end{cases} \dots\dots\dots(4)$$

If M4, M5, M13, M14 work in strong inversion, then I_{out-n} and I_{out-p} are given by (Chiblè, 2000):

$$I_{out-n} = \sqrt{\frac{\beta_{4,5}}{n}} \sqrt{I_{12}} (V_{in} - V_{ref})$$

$$I_{out-p} = \sqrt{\frac{\beta_{13,14}}{n}} \sqrt{I_{12}} (V_{ref} - V_{in})$$

Where V_{in} varies in the range [1.55:1.75]. If the following approximation is assumed:

$$\beta_y \approx \sqrt{\frac{\beta_{4,5}}{n}} \approx \sqrt{\frac{\beta_{13,14}}{n}}$$

Then I_{out-n} and I_{out-p} becomes:

$$I_{out-n} = \beta_y \sqrt{I_{12}} (V_{in} - V_{ref})$$

$$I_{out-p} = \beta_y \sqrt{I_{12}} (V_{ref} - V_{in})$$

By substituting I_{out-n} and I_{out-p} in Eq.(4):

$$I_{out} = \begin{cases} \beta_y \sqrt{I_{12}} (V_{in} - V_{ref}) \xrightarrow{If} V_{ref} < V_w < V_{dd} \\ \beta_y \sqrt{I_{12}} (V_{ref} - V_{in}) \xrightarrow{If} 0 < V_w < V_{ref} \end{cases}$$

By substituting I_{12} “Eq.(3)” in the above equation:

$$I_{out} = \begin{cases} \beta_y \sqrt{\beta_x \times (V_w - V_{ref})^2} (V_{in} - V_{ref}) \xrightarrow{If} V_{ref} < V_w < V_{dd} \\ -\beta_y \sqrt{\beta_x \times (V_w - V_{ref})^2} (V_{ref} - V_{in}) \xrightarrow{If} 0 < V_w < V_{ref} \end{cases}$$

The above equation is simplified as follows:

$$I_{out} = \begin{cases} \beta_y \sqrt{\beta_x} (V_w - V_{ref}) (V_{in} - V_{ref}) \xrightarrow{If} V_{ref} < V_w < V_{dd} \\ -\beta_y \sqrt{\beta_x} (V_w - V_{ref}) (V_{ref} - V_{in}) \xrightarrow{If} 0 < V_w < V_{ref} \end{cases}$$

Or

$$I_{out} = \beta_y \sqrt{\beta_x} (V_w - V_{ref}) (V_{in} - V_{ref}) \xrightarrow{If} 0 < V_w < V_{dd} \dots \dots \dots (5)$$

Eq.(5) represents the multiplication equation of the multiplier circuit, where it is clear the direct multiplication process between the two inputs V_{in} that varies in the range [1.55V: 1.75V] and V_w that varies in the range [0:V_{dd}] and $V_{ref}=1.65V$ is the reference ground voltage.

SIMULATION RESULTS

Circuit dimensions

The dimensions “width and the length” of the MOS transistors have been computed on the base of the technology parameters (e.g. the mobility of the electron, oxide capacitor, etc...). Table 1 shows the designed dimensions (width μm/length μm) of each transistor.

TABLE 1

The Dimensions of the Transistors

M1	M2	M3	M4	M5	M6	M7
1/1	4/8	1/8	3/3	3/3	4/4	4/4
M8	M9	M10	M13	M14	M15	M16
1/1	4/8	4/8	12/3	12/3	4/4	4/4

The dimensions of the transistors are calculated and designed based on the following considerations:

M1, M2, M3 are designed in a way to create $I_1 \approx 0$ when V_w less than or equal to V_{ref} ;

M8, M9, M10 are designed in a way to create $I_2 \approx 0$ when V_w greater than or equal to V_{ref} ;
 M4, M5, M13, M14 are designed in a way to make OTAN and OTAP work in strong inversion region;
 M6, M7, M11, M12, M15, M16 are designed as current mirror;
 The dimensions of the transistors M4 and M5 must be equal;
 The dimensions of the transistors M13, and M14 must be equal;
 The value of the dimensions of the transistors M4, M5 must be different than the dimensions of the M13, and M14 because of the mobility factor, where of the mobility of N-channel transistors are bigger nearly three to four times than the mobility of P-channel transistors.

The silicon area of all transistors in this multiplier is $260 \mu\text{m}^2$, which is lower than in Chiblè (2004) by nearly four times. Including all layout design restrictions and metals area, this area will be little increased. The neuron transistors (Figure 5) are M6, M7, M15, and M16, then the multiplier circuit neuron silicon area is $64 \mu\text{m}^2$, and as result the multiplier circuit synapse silicon area is $196 \mu\text{m}^2$.

Circuit simulation

The proposed circuit have been designed and simulated by using the WinSpice “Wspice3 Simulator for Windows” and by using the spice level 8 and the parameters of a CMOS $0.35\mu\text{m}$ technology. . The current I_{12} versus the input voltage V_w is shown in Figure 2. The output current of the proposed multiplier I_{out} versus the input voltage V_w and the output current I_{out} versus the input voltage V_{in} are shown respectively in Figure 3 and Figure 4:

I_{out} in Figure 3 varies in the range $[-2.5\text{ua}; 2.5\text{ua}]$ and V_w varies in the range $[0; 3.3]$ with step 0.3 and with V_{in} as parameter varies in the range $[1.55; 1.75]$ with step 0.01.

I_{out} in Figure 4 varies in the range $[-2.5\text{ua}; 2.5\text{ua}]$ and V_{in} varies in the range $[1.55; 1.75]$ with step 0.01 and with V_w as parameter varies in the range $[0; 3.3]$ with step 0.3.

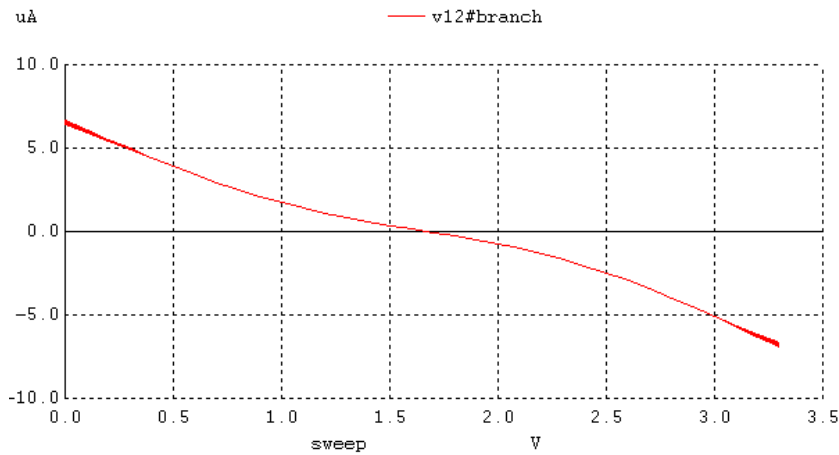


Figure 2. I_{12} versus the input voltage V_w .

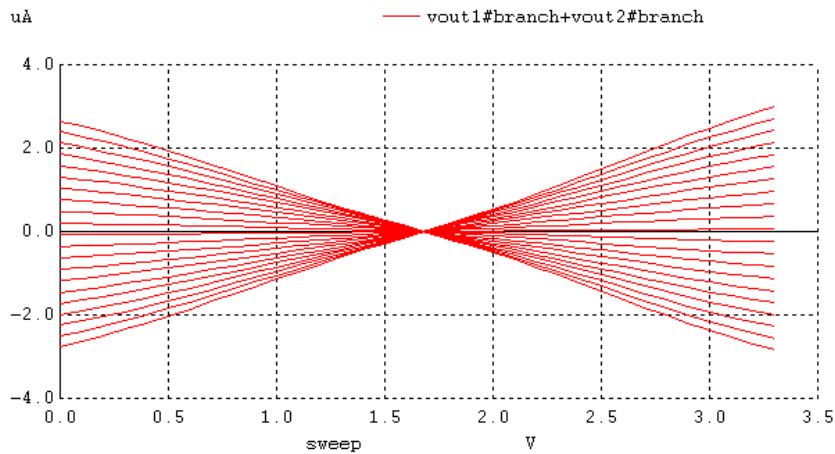


Figure 3. OTANPS simulations - I_{out} versus V_w and with V_{in} as a parameter.

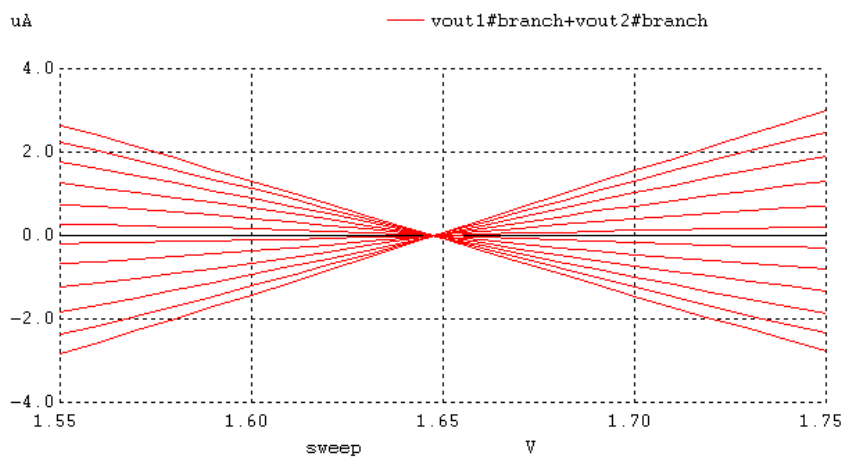


Figure 4. OTANPS simulations - I_{out} versus V_{in} and with V_w as a parameter.

The simulated error due to the mismatch of transistors M3 & M4 and transistors M13 & M14 is equal to 40nA. It is calculated as follows: when the input voltage $V_{in}=1.65V$, the output current $I_{out} = 40nA$, instead of 0nA in the ideal case.

Circuit consumption

The circuit consumption is measured by the Maximum Power Dissipation “MPD” of the circuit, which is given by multiplying the total maximum current I_{max} derived from the power supply voltage V_{dd} times V_{dd} . If OTAN is on or works ($V_w > V_{ref}$) then OTAP is off and vice versa if ($V_w < V_{ref}$), then MPD is given by:

$$MPD = \begin{cases} MPD (M1, M2) + MPD (M6) + MPD (M7) & \xrightarrow{\text{if}} V_w > V_{ref} \\ MPD (M8, M9) + MPD (M10) & \xrightarrow{\text{if}} V_w < V_{ref} \end{cases}$$

Where,

$$MPD (M1, M2) = I_{\max(M1, M2)} * V_{dd};$$

$$MPD (M6) = I_{\max(M6)} * V_{dd};$$

$$MPD (M7) = I_{\max(M7)} * V_{dd};$$

$$MPD (M8, M9) = I_{\max(M8, M9)} * V_{dd};$$

$$MPD (M10) = I_{\max(M10)} * V_{dd};$$

Then MPD becomes:

$$MPD = V_{dd} \begin{cases} I_{\max(M1, M2)} + I_{\max(M6)} + I_{\max(M7)} & \xrightarrow{\text{if}} V_w > V_{ref} \\ I_{\max(M8, M9)} + I_{\max(M10)} & \xrightarrow{\text{if}} V_w < V_{ref} \end{cases} \dots\dots\dots(6)$$

If OTAN is on or works (see Figure 1):

$$\begin{cases} I_{out} = I_4 - I_5 \\ I_{12} = I_4 + I_5 \end{cases} \xrightarrow{\text{then}} I_{out} + I_{12} = 2 * I_4 \xrightarrow{\text{then}} I_4 = \frac{I_{out} + I_{12}}{2}$$

From the current mirror concept:

$$I_{\max(M8, M9)} = I_{\max(M10)}$$

$$I_{\max(M6)} = I_{\max(M7)}$$

$$I_{12} = I_{\max(M1, M2)}$$

Then I₄ is given by:

$$I_4 = I_{\max(M6)} = I_{\max(M7)} = \frac{I_{out} + I_{\max(M1, M2)}}{2}$$

Eq.(6) becomes:

$$MPD = V_{dd} \begin{cases} 2 * I_{\max(M1, M2)} + I_{out} & \xrightarrow{\text{if}} V_w > V_{ref} \\ 2 * I_{\max(M8, M9)} & \xrightarrow{\text{if}} V_w < V_{ref} \end{cases}$$

From the simulation results, V_{dd}=3.3V, I_{max(M1, M2)} = 6μA and I_{out} = 2.5μA, then:

$$MPD = 3.3V \begin{cases} 2 * 6\mu A + 2.5\mu A = 14.5\mu A & \xrightarrow{\text{if}} V_w > V_{ref} \\ 2 * 6\mu A = 12\mu A & \xrightarrow{\text{if}} V_w < V_{ref} \end{cases} = \begin{cases} 47.85\mu W & \xrightarrow{\text{if}} V_w > V_{ref} \\ 39.6\mu W & \xrightarrow{\text{if}} V_w < V_{ref} \end{cases}$$

Finally the MPD of the multiplier circuit is the worst case, which is 47.85μW. If the circuit is divided into synapse and neuron modules, then MPD will be dispersed between them. In synapse will be 39.6μW because:

$$MPD = V_{dd} \begin{cases} I_{\max(M1, M2)} & \xrightarrow{\text{if}} V_w > V_{ref} \\ I_{\max(M8, M9)} + I_{\max(M10)} & \xrightarrow{\text{if}} V_w < V_{ref} \end{cases} = \begin{cases} 19.8\mu W & \xrightarrow{\text{if}} V_w > V_{ref} \\ 39.6\mu W & \xrightarrow{\text{if}} V_w < V_{ref} \end{cases}$$

In neuron will be $28.05\mu W$ because:

$$MPD = V_{dd} \begin{cases} I_{\max(M6)} + I_{\max(M7)} & \text{if } V_w > V_{ref} \\ 0 & \text{if } V_w < V_{ref} \end{cases} = V_{dd} \begin{cases} I_{out} + I_{\max(M1,M2)} & \text{if } V_w > V_{ref} \\ 0 & \text{if } V_w < V_{ref} \end{cases} = \begin{cases} 28.05\mu W & \text{if } V_w > V_{ref} \\ 0\mu W & \text{if } V_w < V_{ref} \end{cases}$$

Comparison

A comparison between the proposed multiplier and the other multipliers are presented and summarized in Table 2. The silicon area and the MPD of the proposed multiplier in this paper will be further reduced; when the circuit is divided into two parts (see next section). The silicon area and MDP become $540\mu m^2$ and $39\mu W$ respectively.

TABLE 2

Comparison between the Proposed Multiplier and the other Multipliers

Multiplier in	Area	MPD
Chiblè (1997)	$6060\mu m^2$	$30\mu w$
Chiblè (2000)	$4900\mu m^2$	$15\mu w$
Chiblè (2004)	$3600\mu m^2$	$14\mu w$
This paper	$720\mu m^2$	$48\mu W$

SYNAPSE AND NEURON IMPLEMENTATION

This section will explain the implementation of the OTANPS proposed multiplier circuit (see Figure 1) in the multi layer perceptron neural networks. Figure 1(b) can be viewed in another way as shown in Figure 5. The synapse part contains 10 transistors and the neuron part contains 4 transistors. They are connected together through three wires metals A, B and C. Figure 6 is the Figure 5 viewed as two black boxes.

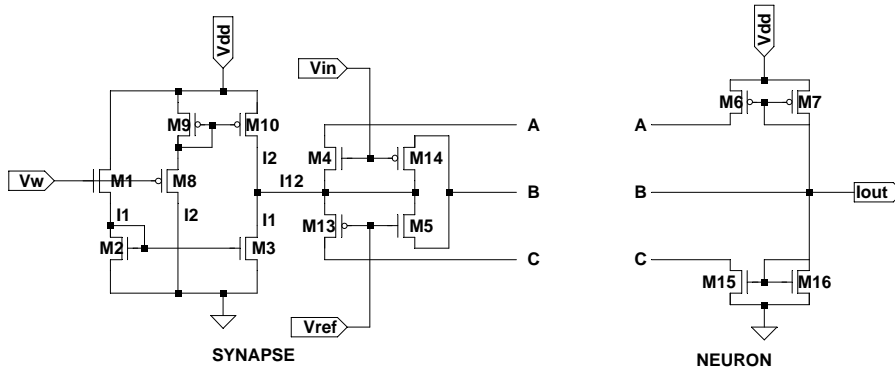


Figure 5. It is Figure 1(b) divided into two parts, one inside the synapse and one inside the neuron.

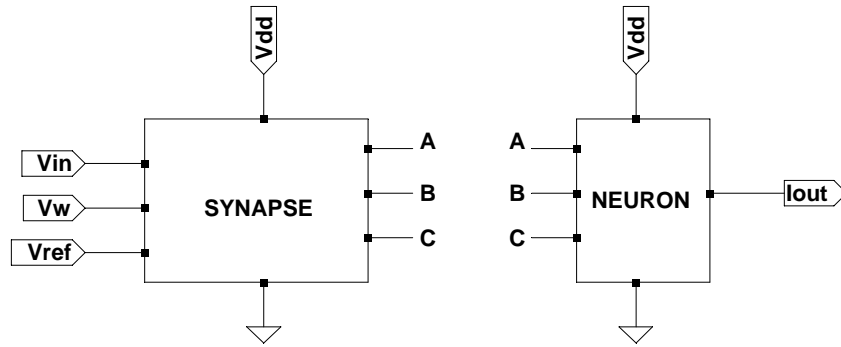


Figure 6. It is Figure 5 viewed as two black boxes.

Figure 7 shows N synapses connected to one neuron. The simulation of one synapse connected to one neuron (I_{out} versus V_w) is shown in Figure 8 and the simulation of five synapses connected to one neuron (I_{out} versus V_w) is shown in Figure 9. It is clear that the values in Figure 9 equals the values in Figure 8 times 5, which is the number of synapses. This will verify the correct operation of the proposed multiplier.

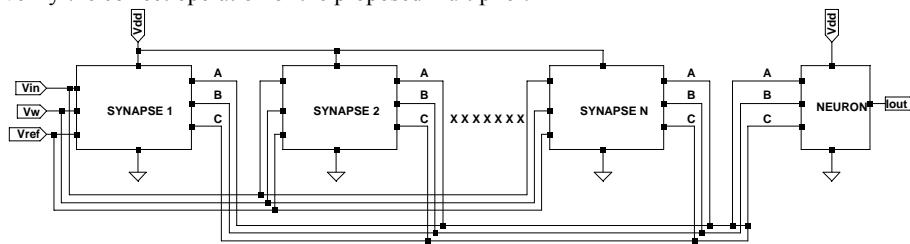


Figure 7. N synapses connected to one neuron.

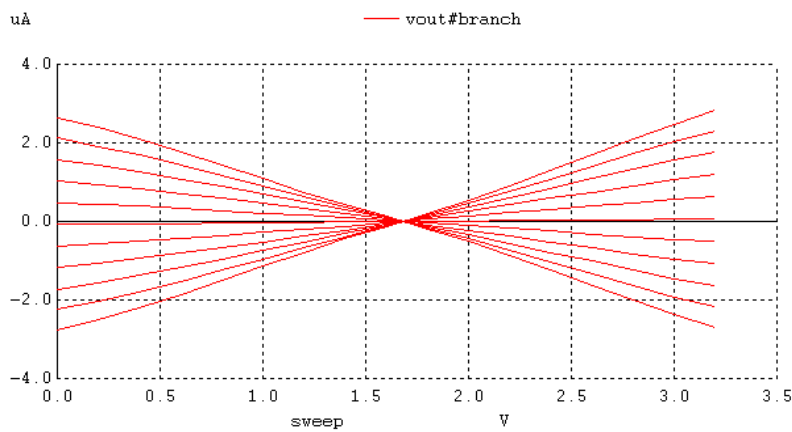


Figure 8. I_{out} versus V_w for one synapse connected to one neuron.

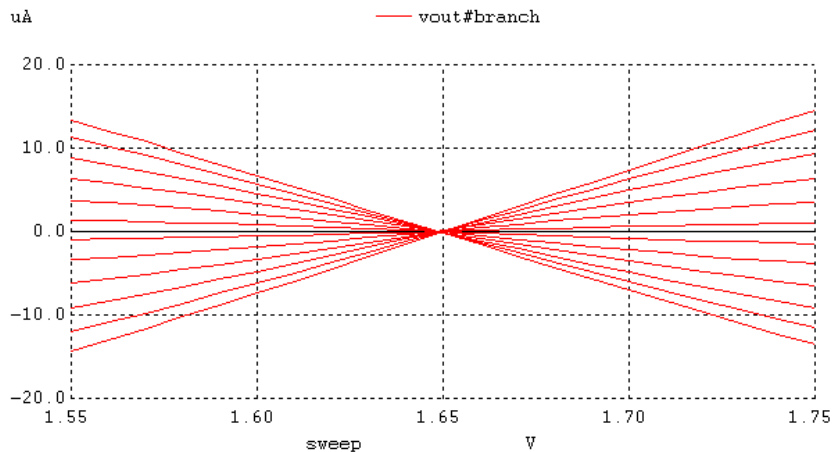


Figure 9. I_{out} versus V_w for five synapses connected to one neuron.

CONCLUSION

In this paper, a new version of four-quadrant analog multiplier has been presented. The proposed multiplier can be used especially in neural networks applications and also in other signal processing operations. The multiplier has small silicon area ($260\mu\text{m}^2$) and low power consumption ($47.85\mu\text{W}$). The power consumption and the silicon area will be further reduced ($196\mu\text{m}^2$ and $39.6\mu\text{W}$ in synapse and $64\mu\text{m}^2$ and $28.05\mu\text{W}$ in neuron), after dividing the circuit into the synapse and neuron modules. The circuit simulation of the multiplier and the circuit simulation inside the synapse and neuron modules have been presented. The future work will be focused on using this multiplier to design and fabricate multi layer perceptron neural network chip.

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REFERENCES

- Bo, G.M., Caviglia, D.D., Chiblè, H. and Valle, M. 1997. Modeling of current switching during the weight update in the analog VLSI implementation of the back propagation algorithm. *International Journal On Advances In Intelligent Systems AMSE*, Special Issue 1997: 91-101.
- Chiblè, H. 1997. *Analysis and design of analog microelectronic neural network architectures with on-chip supervised learning*. Doctoral Dissertation. University of Genoa, Italy.
- Chiblè, H. 2000. Four Quadrant Multiplier for Analog VLSI Neural Networks. *Lebanese Science Journal*, 1(2):51-62.

- Chiblè, H. 2004. Experimental results of an analog VLSI multiplier / synapse / transconductance circuit. *International Journal of Modelling and Simulation*, 24(4): 224-230.
- Chiblè, H. and Ghandour, A. 2007. Different mathematical relations with CMOS VLSI circuits. *Lebanese Science Journal*, 8(1): 75-91.
- Han, G. and Sinencio, E.S. 1998. CMOS transconductance multipliers: A tutorial. *IEEE Trans. on Circuit and Systems: II. Analog and Digital Signal Processing*, 45(12): 1550- 1563.
- Hollis, P.W. and Paulos, J.J. 1990. Artificial neural networks using MOS analog multipliers. *IEEE journal of solid state circuits*, 25(3): 849-855.
- Hopfield, J.J. and Tank, D.W. 1985. Neural computation of decisions in optimization problems. *Biol. Cybern.*, 52:141-152.
- Kapanoglu, B., Yildirim, T. 2004. Low power-four quadrant CMOS analog multiplier for artificial neural networks. *Proceedings of the IEEE 12th Signal Processing and Communications Applications Conference*, 28-30 April 2004, 137-139.
- Kub, F.J., Moon, K.K., Mack, I.A. and Long, F.M. 1990. Programmable analog vector-matrix multipliers. *IEEE Journal of Solid-State Circuits*, 25(1): 207 – 214.
- Lee, S.S., Lau, K.T. and Siek, L. 1995. Four-quadrant CMOS analogue multiplier for artificial neural networks. *Electronic Letters*, 31: 48-49.
- Mead, C.A. 1989. *Analog VLSI and Neural Systems*. Addison-Wesley, Reading.
- Mead, C.A. and Ismail, M. 1989. *Analog VLSI implementation of neural systems*. Boston, Kluwer Academic Publishers.
- Saxen, N. and Clark, J.J. 1994. A four-quadrant CMOS analog multiplier for analog neural networks. *IEEE Journal of Solid-State Circuits*, 29(6): 746 – 749.
- Valle, M., Caviglia, D.D. and Bisio, G.M. 1996. An experimental analog VLSI neural network with on-chip back-propagation learning. *Journal of Analog Integrated Circuits and Signals Processing*, 9: 231-245.
- Vittoz, E.A. 1994. Analog VLSI signal processing: why, where and how? *Journal of VLSI Signal Processing*, 8: 27-44.
- Zhangcai, H., Yasuaki, I., Hong, Y., Quan, Z. 2006. A wide dynamic range four quadrant CMOS analog multiplier using active feedback. *IEEE Asia Pacific Conference on Circuits and Systems*, 4-7 Dec. 2006, 708 – 711.